## **CLAIMS**

## What is claimed is:

- 1 1. A system comprising:
- 2 a first integrated circuit (IC);
- an interface coupled to the first IC; and
- a second IC coupled to the interface, wherein the first IC simultaneously
- 5 transmits the state of each of a plurality of signals not associated with the
- 6 interface to the second IC in-band via the interface each time that a change in the
- 7 state of one of the plurality of signals is detected.
- 1 2. The system of claim 1 wherein the state of all of the plurality of signals is
- 2 sampled at the first IC whenever any of the signals change.
- 1 3. The system of claim 1 wherein the second IC drives each of the signals
- 2 with new values received in-band each time that the plurality of signal values are
- 3 received.
- 1 4. The system of claim 1 wherein the first IC comprises:
- signal logic associated with each of the plurality of signals; and
- 3 protocol logic, coupled to the signal logic associated with each of the
- 4 signals, to transmit the signal values in-band to the protocol to the second IC.
- 1 5. The system of claim 4 wherein the signal logic includes:
- a first flip-flop with an input coupled to an associated signal and an

- 3 output coupled to the protocol logic, the output of the first flip-flop generating a
- 4 held signal value; and
- a second flip-flop having an input coupled to the output of the first flip-
- 6 flop to receive the held signal value, the output of the second flip-flop generating
- 7 a send signal.
- 1 6. The system of claim 4 wherein the signal logic includes:
- a flip-flop with an input coupled to an associated signal and an output
- 3 coupled to the protocol logic, the output of the flip-flop generating a held signal
- 4 value; and
- a counter having an input coupled to the output of the flip-flop to receive
- 6 the held signal value, the output of the second flip-flop generating a send signal.
- 1 7. The system of claim 4 wherein the protocol logic selects a protocol point
- 2 including all of the held signal values simultaneously and integrates the protocol
- 3 point into a protocol that is transmitted to the second IC via the interface.
- 1 8. The system of claim 7 wherein the protocol point being transmitted is
- 2 changed each time an additional signal transitions so that subsequent signal
- 3 transitions are communicated with a short a latency.
- 1 9. The system of claim 1 wherein signal transitions that occur to close to
- 2 previous transitions to be repeated between the first IC and the second IC via the

- 3 interface are discarded and more widely spaced transitions and the steady-state
- 4 value of the signals is repeated.
- 1 10. The system of claim 1 wherein the second IC comprises:
- 2 protocol logic, coupled to the interface, to receive each of the in-band
- 3 signals and to extract the state of each of the in-band signals; and
- 4 sequential logic, coupled to the protocol logic, to maintain the state of each
- 5 of the in-band signals once the state has been received.
- 1 11. A method comprising:
- 2 monitoring the state of each of a plurality of signals at a first integrated
- 3 circuit (IC); and
- 4 transmitting the state of each of the plurality of signals in-band across an
- 5 interface to a second IC each time that a change in the state of one of the plurality
- 6 of signals is detected.
- 1 12. The method of claim 11 wherein monitoring the state of each of a plurality
- of signals at the first IC comprises:
- monitoring a signal held value at protocol logic associated with each of
- 4 the plurality of signals; and
- 5 monitoring a send signal at the protocol logic associated with all of the
- 6 plurality of signals.

- 1 13. The method of claim 12 further comprising:
- selecting a protocol point including all of the held values of the input
- 3 signals simultaneously at the protocol logic: and
- 4 integrating the protocol point into a protocol that is transmitted to the
- 5 second IC via the interface.
- 1 14. The method of claim 13 further comprising:
- 2 receiving the protocol point at the second IC; and
- a extracting the state of each of the plurality of in-band signals.
- 1 15. A system comprising:
- 2 a chipset;
- an interface coupled to the chipset; and
- an integrated circuit (IC) coupled to the chipset, wherein the chipset
- 5 simultaneously transmits the state of each of a plurality of signals not associated
- 6 with the interface to the IC in-band via the interface each time that a change in
- 7 the state of one of the plurality of signals is detected.
- 1 16. The system of claim 15 wherein the state of all of the plurality of signals is
- 2 sampled at the chipset whenever any of the signals change.
- 1 17. The system of claim 15 wherein the IC drives each of the signals with new
- 2 values received in-band each time that the plurality of signal values are received.

- 1 18. The system of claim 15 wherein the chipset comprises:
- signal logic associated with each of the plurality of signals; and
- 3 protocol logic, coupled to the signal logic associated with each of the
- 4 signals, to transmit the signal values in-band to the protocol to the IC.
- 1 19. The system of claim 18 wherein the signal logic includes:
- a first flip-flop with an input coupled to an associated signal and an
- 3 output coupled to the protocol logic, the output of the first flip-flop generating a
- 4 held signal value; and
- 5 a second flip-flop having an input coupled to the output of the first flip-
- 6 flop to receive the held signal value, the output of the second flip-flop generating
- 7 a send signal.
- 1 20. The system of claim 18 wherein the signal logic includes:
- a flip-flop with an input coupled to an associated signal and an output
- 3 coupled to the protocol logic, the output of the flip-flop generating a held signal
- 4 value; and
- 5 a counter having an input coupled to the output of the flip-flop to receive
- 6 the held signal value, the output of the counter generating a send signal.
- 1 21. The system of claim 18 wherein the protocol logic selects a protocol point
- 2 including all of the held signal values simultaneously and integrates the protocol

- 3 point into a protocol that is transmitted to the IC via the interface.
- 1 22. The system of claim 21 wherein the protocol point being transmitted is
- 2 changed each time a held signal transitions so that subsequent signal transitions
- 3 are communicated with a short a latency.
- 1 23. The system of claim 15 wherein signal transitions that occur to close to
- 2 previous transitions to be repeated between the chipset and the IC via the
- 3 interface are discarded and more widely spaced transitions and the steady-state
- 4 value of the signals is repeated.
- 1 24. The system of claim 15 wherein the IC comprises:
- 2 protocol logic, coupled to the interface, to receive each of the in-band
- 3 signals and to extract the state of each of the in-band signals; and
- 4 sequential logic, coupled to the protocol logic, to maintain the state of each
- 5 of the in-band signals once the state has been received.